What is claimed is:

1. A semiconductor device having at least a solder bump formed of alloy solder on an under-bump layer including first metal formed on a wiring layer, comprising:

an intermetallic compound including metal that is a main component of the alloy solder and second metal different from the metal that is the main component of the alloy solder, wherein the intermetallic compound is formed between the solder bump and the under-bump layer.

2. A semiconductor device having at least a solder bump formed of alloy solder on an under-bump layer including first metal formed on a wiring layer, comprising:

an alloy layer composed of a combination of an intermetallic compound of metal that is a main component of the alloy solder and second metal different from the metal that is the main component of the alloy solder, and an intermetallic compound of the first metal included in the under-bump layer and the metal that is the main component of the alloy solder, wherein the alloy layer is formed between the solder bump and the under-bump layer.

3. A semiconductor device having at least a solder bump formed of alloy solder on an under-bump layer including first metal formed on a wiring layer, comprising:

an intermetallic compound formed between the solder bump

and the under-bump layer, wherein the intermetallic compound includes:

second metal constituting a metal layer that is temporarily arranged on the under-bump layer and is then dissolved into the alloy solder on formation of the solder bump; and

metal that is a main component of the alloy solder.

4. A semiconductor device having at least a solder bump formed of alloy solder on an under-bump layer including first metal formed on a wiring layer, comprising:

an alloy layer formed between the solder bump and the under-bump layer, wherein the alloy layer is composed of a combination of:

an intermetallic compound composed of second metal constituting a metal layer that is temporarily arranged on the under-bump layer and is then dissolved into the alloy solder on formation of the solder bump, and metal that is a main component of the alloy solder; and

an intermetallic compound of the first metal included in the under-bump layer and the metal that is the main component of the alloy solder.

5. The semiconductor device according to claim 1, wherein the metal that is the main component of the alloy solder is tin.

6. The semiconductor device according to claim 2, wherein the metal that is the main component of the alloy solder is tin.

7. The semiconductor device according to claim 3, wherein the

metal that is the main component of the alloy solder is tin.

8. The semiconductor device according to claim 4, wherein the metal that is the main component of the alloy solder is tin.

9. The semiconductor device according to claim 5, wherein metal that is a second main component of the alloy solder after the tin is silver.

10. The semiconductor device according to claim 6, wherein metal that is a second main component of the alloy solder after the tin is silver.

11. The semiconductor device according to claim 7, wherein metal that is a second main component of the alloy solder after the tin is silver.

12. The semiconductor device according to claim 8, wherein metal that is a second main component of the alloy solder after the tin is silver.

13. The semiconductor device of claim 5, wherein copper is added to the alloy solder.

14. The semiconductor device of claim 6, wherein copper is added to the alloy solder.

15. The semiconductor device of claim 7, wherein copper is added to the alloy solder.

16. The semiconductor device of claim 8, wherein copper is added to the alloy solder.

17. The semiconductor device of claim 9, wherein copper is added to the alloy solder.

18. The semiconductor device of claim 10, wherein copper is added to the alloy solder.

19. The semiconductor device of claim 11, wherein copper is added to the alloy solder.

20. The semiconductor device of claim 12, wherein copper is added to the alloy solder.

21. The semiconductor device according to claim 1, wherein the second metal is a metal which is different from the first metal and is allowed to form an intermetallic compound with tin.

22. The semiconductor device according to claim 21, wherein the second metal is copper.

23. The semiconductor device according to claim 2, wherein the second metal is a metal which is different from the first metal and is allowed to form an intermetallic compound with tin.

24. The semiconductor device according to claim 23, wherein the second metal is copper.

25. The semiconductor device according to claim 3, wherein the second metal is a metal which is different from the first metal and is allowed to form an intermetallic compound with tin.

26. The semiconductor device according to claim 25, wherein the second metal is copper.

27. The semiconductor device according to claim 4, wherein the second metal is a metal which is different from the first metal and is allowed to form an intermetallic compound with tin.

28. The semiconductor device according to claim 27, wherein the second metal is copper.

29. The semiconductor device according to claim 1, wherein the first metal included in the under-bump layer includes nickel.

30. The semiconductor device according to claim 29, wherein the under-bump layer is a laminated film formed from one of nickel and nickel

alloy with different film qualities.

31. The semiconductor device according to claim 29, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy and one of copper and copper alloy.

32. The semiconductor device according to claim 30, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

33. The semiconductor device according to claim 31, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

34. The semiconductor device according to claim 2, wherein the first metal included in the under-bump layer includes nickel.

35. The semiconductor device according to claim 34, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy with different film qualities.

36. The semiconductor device according to claim 34, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy and one of copper and copper alloy.

37. The semiconductor device according to claim 35, wherein the

nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

38. The semiconductor device according to claim 36, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

39. The semiconductor device according to claim 3, wherein the first metal included in the under-bump layer includes nickel.

40. The semiconductor device according to claim 39, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy with different film qualities.

41. The semiconductor device according to claim 39, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy and one of copper and copper alloy.

42. The semiconductor device according to claim 40, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

43. The semiconductor device according to claim 41, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

44. The semiconductor device according to claim 4, wherein the first metal included in the under-bump layer includes nickel.

45. The semiconductor device according to claim 44, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy with different film qualities.

46. The semiconductor device according to claim 44, wherein the under-bump layer is a laminated film formed from one of nickel and nickel alloy and one of copper and copper alloy.

47. The semiconductor device according to claim 45, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

48. The semiconductor device according to claim 46, wherein the nickel alloy includes one selected from a group consisting of nickel/vanadium alloy, nickel/phosphorous alloy and nickel titanium alloy.

49. The semiconductor device according to claim 1, wherein a contact layer is provided between the wiring layer and the under-bump layer.

50. The semiconductor device of claim 49, wherein the contact layer includes one of titanium and titanium/tungsten alloy.

51. The semiconductor device according to claim 2, wherein a contact layer is provided between the wiring layer and the under-bump layer.

52. The semiconductor device of claim 51, wherein the contact layer includes one of titanium and titanium/tungsten alloy.

53. The semiconductor device according to claim 3, wherein a contact layer is provided between the wiring layer and the under-bump layer.

54. The semiconductor device of claim 53, wherein the contact layer includes one of titanium and titanium/tungsten alloy.

55 The semiconductor device according to claim 4, wherein a contact layer is provided between the wiring layer and the under-bump layer.

56. The semiconductor device of claim 55, wherein the contact layer includes one of titanium and titanium/tungsten alloy.

57. A method for manufacturing a semiconductor device comprising at least a solder bump of alloy solder formed on a wiring layer via an under-bump layer including first metal, comprising the steps of:

fusing alloy solder having second metal different from main component metal of the solder bump added thereto; and

cooling the fused alloy solder to deposit an intermetallic compound including the second metal and the main component metal of the alloy solder at an interface between the under-bump layer and the solder bump.

58. A method for manufacturing a semiconductor device, comprising the steps of:

forming, on a wiring layer, an under-bump layer including first metal which is to form a first intermetallic compound at an interface through reaction with alloy solder;

supplying alloy solder having second metal different from main component metal added thereto; and

forming an alloy layer at an interface between the under-bump layer and the alloy solder by temporary fusing the alloy solder before cooling, wherein the alloy layer is a combination of the first intermetallic compound and a second intermetallic compound of the main component metal of the alloy solder and the second metal.

59. A method for manufacturing a semiconductor device with at least a solder bump made of alloy solder formed on a wiring layer via an under-bump layer including first metal, comprising the steps of:

forming a metal layer of second metal on the under-bump layer; and

when forming the solder bump, fusing the entire metal layer into the alloy solder and then cooling it to deposit an intermetallic compound including the second metal and the main component metal of the

alloy solder at an interface between the under-bump layer and the solder bump.

60. A semiconductor device manufacturing method, comprising the steps of:

forming, on a wiring layer, an under-bump layer, including first metal which is to form a first intermetallic compound at an interface through reaction with alloy solder;

forming a metal layer made of second metal which is to form a second intermetallic compound through reaction with the alloy solder;

supplying the alloy solder; and

forming an alloy layer at an interface between the under-bump layer and the alloy solder by cooling after temporary fusing of the alloy solder, wherein the alloy layer is a combination of the first intermetallic compound and the second intermetallic compound.

61. The semiconductor device manufacturing method according to claim 59, wherein an oxidation prevention film made of gold is further thinly formed on the metal layer.

62. The semiconductor device manufacturing method according to claim 60, wherein an oxidation prevention film made of gold is further thinly formed on the metal layer.

63. A semiconductor device manufacturing method, comprising the steps of:

forming, on a wiring layer, an under-bump layer including first metal which is to form a first intermetallic compound at an interface through reaction with alloy solder;

forming a metal layer made of second metal which is to form a second intermetallic compound through reaction with the alloy solder;

forming a thin film of tin on the metal layer and forming an alloy layer of the second metal and the tin; and

supplying the alloy solder.

64. The semiconductor device manufacturing method according to claim 57, further comprising the step of, before forming the under-bump layer on the wiring layer, forming a contact layer for maintaining adhesion of the wiring layer and the under-bump layer.

65. The semiconductor device manufacturing method according to claim 58, further comprising the step of, before forming the under-bump layer on the wiring layer, forming a contact layer for maintaining adhesion of the wiring layer and the under-bump layer.

66. The semiconductor device manufacturing method according to claim 59, further comprising the step of, before forming the under-bump layer on the wiring layer, forming a contact layer for maintaining adhesion of the wiring layer and the under-bump layer.

67. The semiconductor device manufacturing method according to claim 60, further comprising the step of, before forming the under-bump

layer on the wiring layer, forming a contact layer for maintaining adhesion of the wiring layer and the under-bump layer.

68. The semiconductor device manufacturing method according to claim 63, further comprising the step of, before forming the under-bump layer on the wiring layer, forming a contact layer for maintaining adhesion of the wiring layer and the under-bump layer.

69. The semiconductor device manufacturing method according to claim 57, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by setting a temperature of an interface of the solder bump with the under-bump layer to lower than a temperature at the top of the solder bump on a specified temperature gradient.

70. The semiconductor device manufacturing method according to claim 58, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by setting a temperature of an interface of the solder bump with the under-bump layer to lower than a temperature at the top of the solder bump on a specified temperature gradient.

71. The semiconductor device manufacturing method according to claim 59, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by setting a temperature of an interface of the solder bump with the

under-bump layer to lower than a temperature at the top of the solder bump on a specified temperature gradient.

72. The semiconductor device manufacturing method according to claim 60, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by setting a temperature of an interface of the solder bump with the under-bump layer to lower than a temperature at the top of the solder bump on a specified temperature gradient.

73. The semiconductor device manufacturing method according to claim 63, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by setting a temperature of an interface of the solder bump with the under-bump layer to lower than a temperature at the top of the solder bump on a specified temperature gradient.

74. The semiconductor device manufacturing method according to claim 57, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by mounting the semiconductor device on a stage and causing a heating plate and a cooling plate movably provided at a lower part of the stage to be sequentially brought into contact with the stage.

75. The semiconductor device manufacturing method according to claim 58, wherein, when forming the solder bump, fusing of the alloy

solder and deposition of the intermetallic compound are carried out by mounting the semiconductor device on a stage and causing a heating plate and a cooling plate movably provided at a lower part of the stage to be sequentially brought into contact with the stage.

76. The semiconductor device manufacturing method according to claim 59, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by mounting the semiconductor device on a stage and causing a heating plate and a cooling plate movably provided at a lower part of the stage to be sequentially brought into contact with the stage.

77. The semiconductor device manufacturing method according to claim 60, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by mounting the semiconductor device on a stage and causing a heating plate and a cooling plate movably provided at a lower part of the stage to be sequentially brought into contact with the stage.

78. The semiconductor device manufacturing method according to claim 63, wherein, when forming the solder bump, fusing of the alloy solder and deposition of the intermetallic compound are carried out by mounting the semiconductor device on a stage and causing a heating plate and a cooling plate movably provided at a lower part of the stage to be sequentially brought into contact with the stage.

79. The semiconductor device manufacturing method according to claim 74, wherein, at the time of heating using the heating plate, the semiconductor device is also heated from above by a non-contact heater provided at an upper part of the semiconductor device, and at the time of cooling using the cooling plate, while continuing heating using the non-contact heater, a temperature gradient between the top of solder bump and the interface of the solder bump with the under-bump layer is increased to promote deposition to the interface of the intermetallic compound with the under-bump layer.

80. The semiconductor device manufacturing method according to claim 75, wherein, at the time of heating using the heating plate, the semiconductor device is also heated from above by a non-contact heater provided at an upper part of the semiconductor device, and at the time of cooling using the cooling plate, while continuing heating using the non-contact heater, a temperature gradient between the top of solder bump and the interface of the solder bump with the under-bump layer is increased to promote deposition to the interface of the intermetallic compound with the under-bump layer.

81. The semiconductor device manufacturing method according to claim 76, wherein, at the time of heating using the heating plate, the semiconductor device is also heated from above by a non-contact heater provided at an upper part of the semiconductor device, and at the time of cooling using the cooling plate, while continuing heating using the non-contact heater, a temperature gradient between the top of solder bump

and the interface of the solder bump with the under-bump layer is increased to promote deposition to the interface of the intermetallic compound with the under-bump layer.

82. The semiconductor device manufacturing method according to claim 77, wherein, at the time of heating using the heating plate, the semiconductor device is also heated from above by a non-contact heater provided at an upper part of the semiconductor device, and at the time of cooling using the cooling plate, while continuing heating using the non-contact heater, a temperature gradient between the top of solder bump and the interface of the solder bump with the under-bump layer is increased to promote deposition to the interface of the intermetallic compound with the under-bump layer.

83. The semiconductor device manufacturing method according to claim 78, wherein, at the time of heating using the heating plate, the semiconductor device is also heated from above by a non-contact heater provided at an upper part of the semiconductor device, and at the time of cooling using the cooling plate, while continuing heating using the non-contact heater, a temperature gradient between the top of solder bump and the interface of the solder bump with the under-bump layer is increased to promote deposition to the interface of the intermetallic compound with the under-bump layer.

84. The semiconductor device manufacturing method according to claim 74, wherein cooling using the cooling plate is carried out at cooling

rate of at least 2℃ per second.

85. The semiconductor device manufacturing method according to claim 75, wherein cooling using the cooling plate is carried out at cooling rate of at least 2℃ per second.

86. The semiconductor device manufacturing method according to claim 76, wherein cooling using the cooling plate is carried out at cooling rate of at least 2℃ per second.

87. The semiconductor device manufacturing method according to claim 77, wherein cooling using the cooling plate is carried out at cooling rate of at least 2℃ per second.

88. The semiconductor device manufacturing method according to claim 78, wherein cooling using the cooling plate is carried out at cooling rate of at least 2℃ per second.

89. The semiconductor device manufacturing method according to claim 74, wherein the heating using the heating plate and the cooling using the cooling plate are carried out under a vacuum atmosphere of a specified gas.

90. The semiconductor device manufacturing method according to claim 75, wherein the heating using the heating plate and the cooling using the cooling plate are carried out under a vacuum atmosphere of a

specified gas.

91. The semiconductor device manufacturing method according to claim 76, wherein the heating using the heating plate and the cooling using the cooling plate are carried out under a vacuum atmosphere of a specified gas.

92. The semiconductor device manufacturing method according to claim 77, wherein the heating using the heating plate and the cooling using the cooling plate are carried out under a vacuum atmosphere of a specified gas.

93. The semiconductor device manufacturing method according to claim 78, wherein the heating using the heating plate and the cooling using the cooling plate are carried out under a vacuum atmosphere of a specified gas.

94. The semiconductor device manufacturing method according to claim 89, wherein the specified gas includes one of an inert gas and a reductive gas.

95. The semiconductor device manufacturing method according to claim 90, wherein the specified gas includes one of an inert gas and a reductive gas.

96. The semiconductor device manufacturing method according

to claim 91, wherein the specified gas includes one of an inert gas and a reductive gas.

97. The semiconductor device manufacturing method according to claim 92, wherein the specified gas includes one of an inert gas and a reductive gas.

98. The semiconductor device manufacturing method according to claim 93, wherein the specified gas includes one of an inert gas and a reductive gas.

99. The semiconductor device manufacturing method according to claim 94, wherein the inert gas comprises one of nitrogen and argon, and the reductive gas comprises one of hydrogen and a mixed gas including hydrogen.

100. The semiconductor device manufacturing method according to claim 95, wherein the inert gas comprises one of nitrogen and argon, and the reductive gas comprises one of hydrogen and a mixed gas including hydrogen.

101. The semiconductor device manufacturing method according to claim 96, wherein the inert gas comprises one of nitrogen and argon, and the reductive gas comprises one of hydrogen and a mixed gas including hydrogen.

102. The semiconductor device manufacturing method according to claim 97, wherein the inert gas comprises one of nitrogen and argon, and the reductive gas comprises one of hydrogen and a mixed gas including hydrogen.

103. The semiconductor device manufacturing method according to claim 98, wherein the inert gas comprises one of nitrogen and argon, and the reductive gas comprises one of hydrogen and a mixed gas including hydrogen.

104. The semiconductor device manufacturing method according to claim 57, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by sputtering.

105. The semiconductor device manufacturing method according to claim 58, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by sputtering.

106. The semiconductor device manufacturing method according to claim 59, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed

by sputtering.

107. The semiconductor device manufacturing method according to claim 60, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by sputtering.

108. The semiconductor device manufacturing method according to claim 63, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by sputtering.

109. The semiconductor device manufacturing method according to claim 57, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

110. The semiconductor device manufacturing method according to claim 58, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

111. The semiconductor device manufacturing method according to claim 59, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

112. The semiconductor device manufacturing method according to claim 60, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

113. The semiconductor device manufacturing method according to claim 63, wherein the under-bump layer is formed from one of a single film and a laminate of a plurality of films made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

114. The semiconductor device manufacturing method according to claim 57, wherein the under-bump layer is formed as a laminate film of a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by the spattering and a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

115. The semiconductor device manufacturing method according to claim 58, wherein the under-bump layer is formed as a laminate film of a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by the spattering and a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

116. The semiconductor device manufacturing method according to claim 59, wherein the under-bump layer is formed as a laminate film of a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by the spattering and a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

117. The semiconductor device manufacturing method according to claim 60, wherein the under-bump layer is formed as a laminate film of a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by the spattering and a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

118. The semiconductor device manufacturing method according to claim 63, wherein the under-bump layer is formed as a laminate film of a

film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by the spattering and a film made of one selected from a group consisting of nickel, nickel alloy, copper and copper alloy which are formed by one of nonelectrolytic plating and electrolytic plating.

119. The semiconductor device manufacturing method according to claim 59, wherein the metal layer includes a copper thin film formed by at least one of sputtering, nonelectrolytic plating, and electrolytic plating.

120. The semiconductor device manufacturing method according to claim 60, wherein the metal layer includes a copper thin film formed by at least one of sputtering, nonelectrolytic plating, and electrolytic plating.

121. The semiconductor device manufacturing method according to claim 63, wherein the metal layer includes a copper thin film formed by at least one of sputtering, nonelectrolytic plating, and electrolytic plating.

122. The semiconductor device manufacturing method according to claim 119, wherein a film thickness of the metal layer is set so that the metal layer fuses totally into the alloy solder when fusing the alloy solder, and, when cooling the alloy solder, at least some of metal of the metal layer is deposited from the alloy solder.

123. The semiconductor device manufacturing method according to claim 120, wherein a film thickness of the metal layer is set so that the

metal layer fuses totally into the alloy solder when fusing the alloy solder, and, when cooling the alloy solder, at least some of metal of the metal layer is deposited from the alloy solder.

124. The semiconductor device manufacturing method according to claim 121, wherein a film thickness of the metal layer is set so that the metal layer fuses totally into the alloy solder when fusing the alloy solder, and, when cooling the alloy solder, at least some of metal of the metal layer is deposited from the alloy solder.

125. The semiconductor device manufacturing method according to claim 57, wherein the alloy solder is supplied as one of a ball and pellet formed to a specified amount.

126. The semiconductor device manufacturing method according to claim 58, wherein the alloy solder is supplied as one of a ball and pellet formed to a specified amount.

127. The semiconductor device manufacturing method according to claim 59, wherein the alloy solder is supplied as one of a ball and pellet formed to a specified amount.

128. The semiconductor device manufacturing method according to claim 60, wherein the alloy solder is supplied as one of a ball and pellet formed to a specified amount.

129. The semiconductor device manufacturing method according to claim 63, wherein the alloy solder is supplied as one of a ball and pellet formed to a specified amount.

130. The semiconductor device manufacturing method according to claim 57, wherein the alloy solder is supplied as solder paste.

131. The semiconductor device manufacturing method according to claim 58, wherein the alloy solder is supplied as solder paste.

132. The semiconductor device manufacturing method according to claim 59, wherein the alloy solder is supplied as solder paste.

133. The semiconductor device manufacturing method according to claim 60, wherein the alloy solder is supplied as solder paste.

134. The semiconductor device manufacturing method according to claim 63, wherein the alloy solder is supplied as solder paste.

135. The semiconductor device manufacturing method according to claim 57, wherein the main component of the alloy solder is tin.

136. The semiconductor device manufacturing method according to claim 58, wherein the main component of the alloy solder is tin.

137. The semiconductor device manufacturing method according

to claim 59, wherein the main component of the alloy solder is tin.

138. The semiconductor device manufacturing method according to claim 60, wherein the main component of the alloy solder is tin.

139. The semiconductor device manufacturing method according to claim 63, wherein the main component of the alloy solder is tin.

140. The semiconductor device manufacturing method according to claim 135, wherein a second main component of the alloy solder after tin is silver.

141. The semiconductor device manufacturing method according to claim 136, wherein a second main component of the alloy solder after tin is silver.

142. The semiconductor device manufacturing method according to claim 137, wherein a second main component of the alloy solder after tin is silver.

143. The semiconductor device manufacturing method according to claim138. wherein a second main component of the alloy solder after tin is silver.

144. The semiconductor device manufacturing method according to claim 139, wherein a second main component of the alloy solder after tin

is silver.

145. The semiconductor device manufacturing method according to claim 135, wherein copper is added to the alloy solder.

146. The semiconductor device manufacturing method according to claim 136, wherein copper is added to the alloy solder.

147. The semiconductor device manufacturing method according to claim 137, wherein copper is added to the alloy solder.

148. The semiconductor device manufacturing method according to claim138, wherein copper is added to the alloy solder.

149. The semiconductor device manufacturing method according to claim 139, wherein copper is added to the alloy solder.

150. A semiconductor manufacturing apparatus comprising:
a stage for mounting a sample;
a heating section for heating the sample; and
a cooling section for cooling the sample from below.

151. The semiconductor manufacturing apparatus according to claim 150, wherein the sample is a semiconductor device having solder.

152. The semiconductor manufacturing apparatus according to

claim 150, wherein the heating section comprises a heating plate with a built-in heater, the cooling section comprises a cooling plate with a built-in cooling medium, wherein heating and cooling are carried out by sequentially bringing the heating plate and the cooling plate into contact with a lower surface of the stage to conduct heat.

153. The semiconductor manufacturing apparatus according to claim 150, wherein at least one of the heating section and the cooling section is built-in to the stage.

154. The semiconductor manufacturing apparatus according to claim 150, further comprising:

a non-contact heating section provided at an upper part of the stage, for heating the sample from above without contact.

155. The semiconductor manufacturing apparatus according to claim 151, further comprising:

a non-contact heating section provided at an upper part of the stage, for heating the semiconductor device from above without contact.

156. The semiconductor manufacturing apparatus according to claim 154, further comprising:

a temperature sensor for measuring a temperature of the stage and a surface of the sample, and

a controller for independently controlling the cooling section and the non-contact heating section by reference to an output from the

temperature sensor so that a temperature gradient of an upper surface and a lower surface of the sample becomes a specified value.

157. The semiconductor manufacturing apparatus according to claim 155, further comprising:

a temperature sensor for measuring a temperature of the stage and a surface of the semiconductor device, and

a controller for independently controlling the cooling section and the non-contact heating section by reference to an output from the temperature sensor so that a temperature gradient of an upper surface and a lower surface of the semiconductor device becomes a specified value.

158. An electrode structure comprising:

an under-bump layer;

a solder bump; and

an intermetallic compound formed between the under-bump layer and the solder bump.